FIG. 1

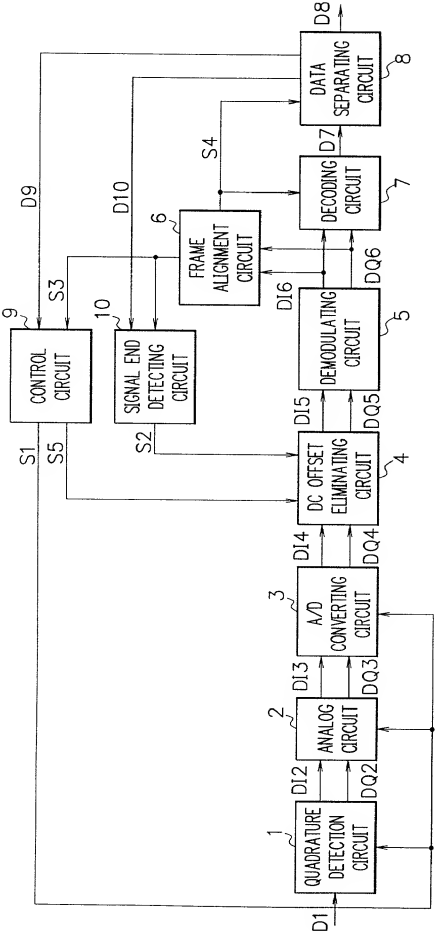
D1
QUADRATURE DETECTION CIRCUIT
1
DI2
DQ2
ANALOG CIRCUIT
2
DI3
DQ3
A/D CONVERTING CIRCUIT
3
DI4
DQ4
DC OFFSET ELIMINATING CIRCUIT
4
DI5
DQ5
DEMODULATING CIRCUIT
5
DI6
DQ6
FRAME ALIGNMENT CIRCUIT
6
D7
DECODING CIRCUIT
7
D8
DATA SEPARATING CIRCUIT
8
D9
CONTROL CIRCUIT
9
S1
S3
D10
SIGNAL END DETECTING CIRCUIT
10
S2
S4
S5

FIG. 2

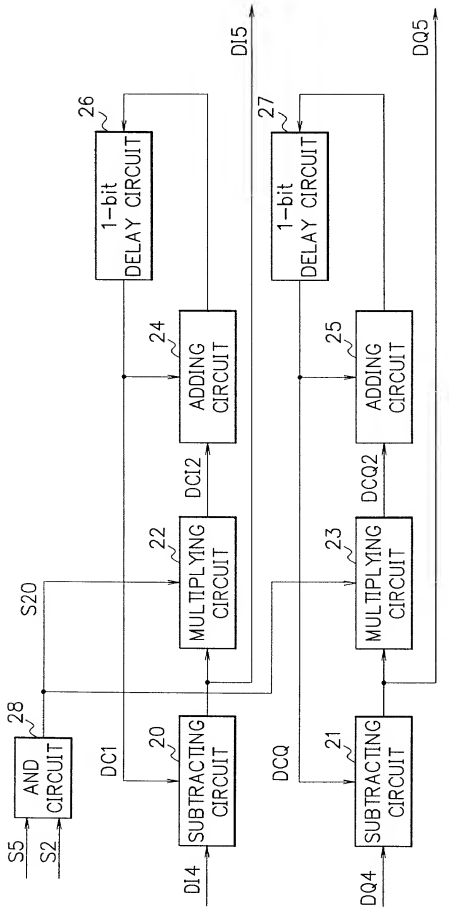
S5
S2
AND CIRCUIT
28
S20
DI4
SUBTRACTING CIRCUIT
20
DC1
MULTIPLYING CIRCUIT
22
DCI2
ADDING CIRCUIT
24
1-bit DELAY CIRCUIT
26
DI5
DCQ
SUBTRACTING CIRCUIT
21
MULTIPLYING CIRCUIT
23
DCQ2
ADDING CIRCUIT
25
1-bit DELAY CIRCUIT
27
DQ4
DQ5

FIG. 3

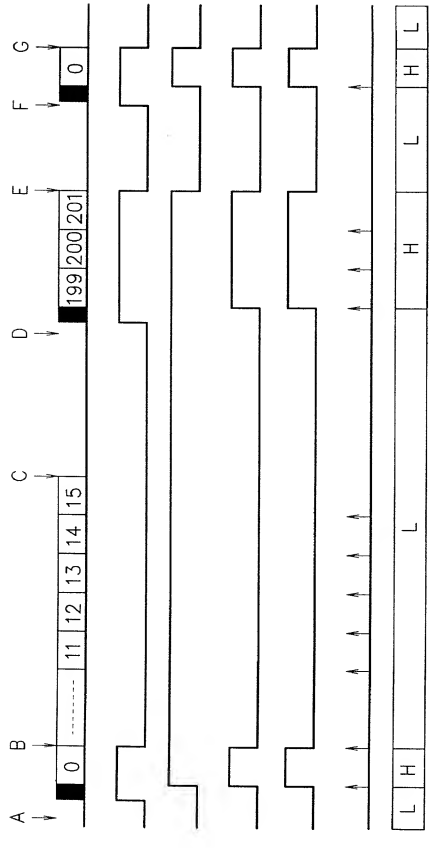

FIG. 4 PRIOR ART

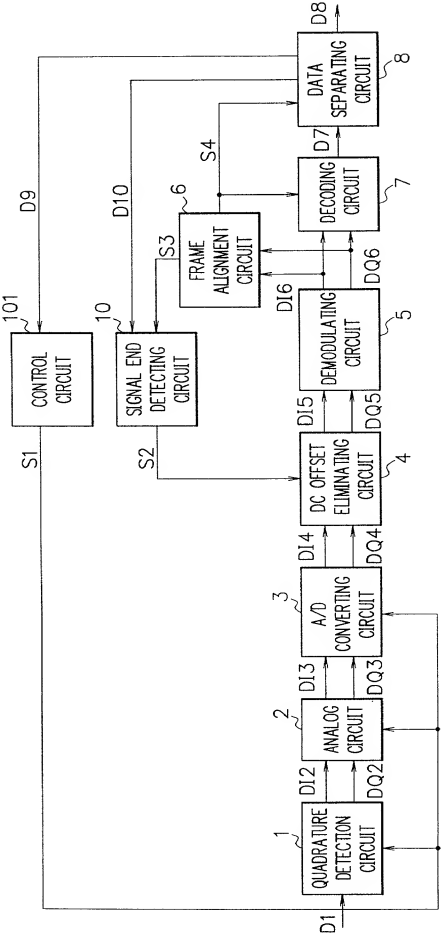

FIG. 5 PRIOR ART

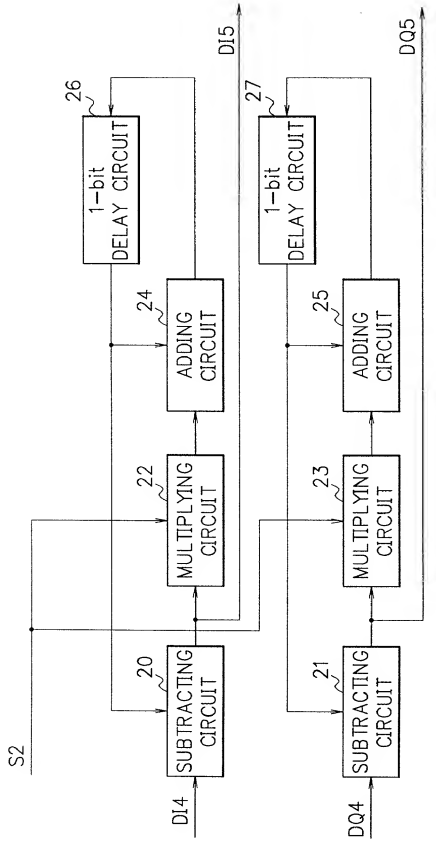

FIG. 6

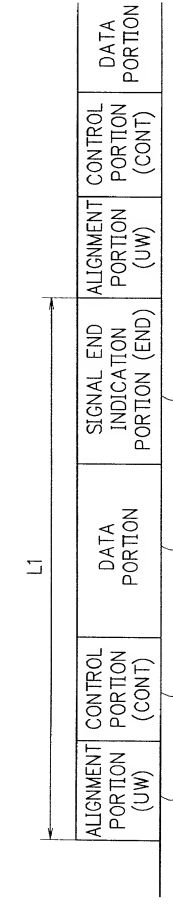
L1
ALIGNMENT PORTION (UW)
CONTROL PORTION (CONT)
DATA PORTION
SIGNAL END INDICATION PORTION (END)
ALIGNMENT PORTION (UW)
CONTROL PORTION (CONT)
DATA PORTION
61
62
63
64

FIG. 7

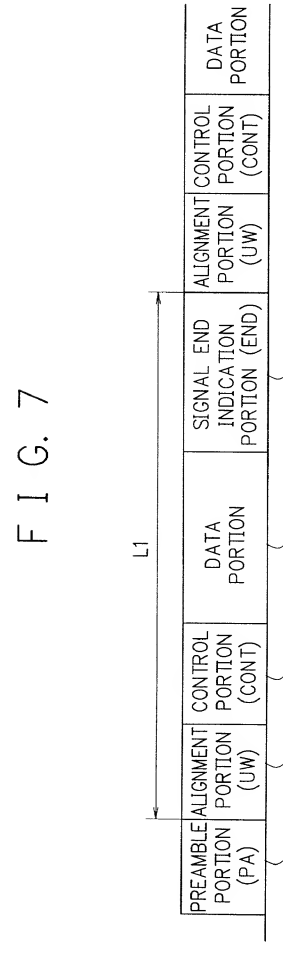
L1
PREAMBLE PORTION (PA)
ALIGNMENT PORTION (UW)
CONTROL PORTION (CONT)
DATA PORTION
SIGNAL END INDICATION PORTION (END)
ALIGNMENT PORTION (UW)
CONTROL PORTION (CONT)
DATA PORTION
70
71
72
73
74

FIG. 8 PRIOR ART

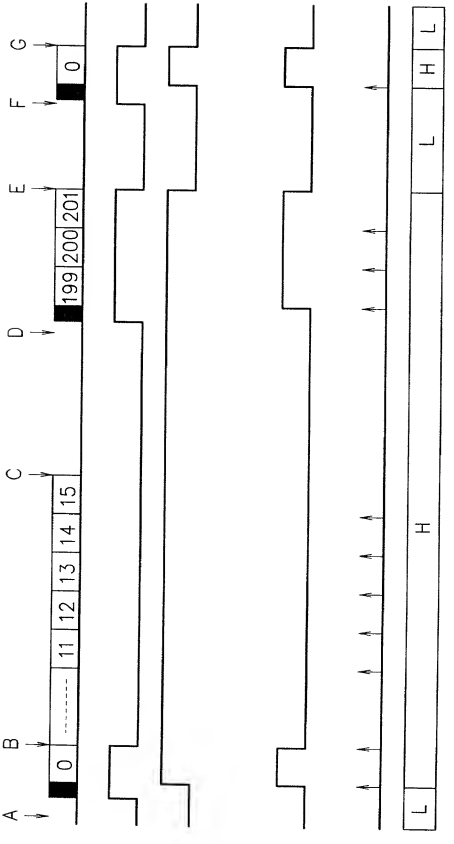

FIG. 9

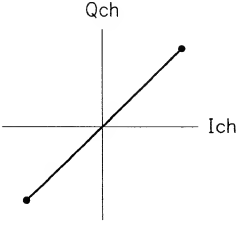
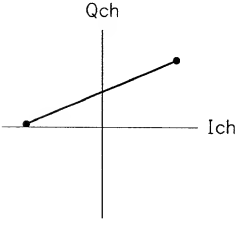
FIG. 10